WHAT IS CLAIMED IS:

1. A circuit for converting voltage levels comprising:

a first power supply providing a first voltage level;

a second power supply providing a second voltage level;

a first transistor formed between the first and second power supplies including a gate electrode for receiving an input signal including a first state and a second state;

a second transistor formed between the first transistor and the second power supply including a gate electrode for receiving a bias voltage; and

a current source formed between the second transistor and the second power supply providing a current in response to the first state of the input signal;

wherein a voltage level at a node disposed between the second transistor and the current source is pulled to a third voltage level in response to the first state of the input signal, and pulled to the second voltage level in response to the second state of the input signal.

2. The circuit of claim 1, the first and second transistors further comprising high-voltage transistors.

3. The circuit of claim 1, the first transistor further comprising an electrode coupled to the first power supply.

4. The circuit of claim 1, the second transistor further comprising an electrode coupled to the current source.

5. The circuit of claim 1, the bias voltage clamping the voltage level at the node between the second and third voltage levels.

6. The circuit of claim 5, the bias voltage being approximately the third voltage level plus a gate-to-source voltage of the second transistor.

7. The circuit of claim 1 further comprising a complementary inverter coupled between a third power supply providing the third voltage level and the second power supply.

8. The circuit of claim 7, the complementary inverter further comprising:

a third transistor including a gate electrode coupled to the node; and

a fourth transistor coupled in series with the third transistor including a gate electrode coupled to the node.

9. The circuit of claim 8, the third transistor further comprising an electrode coupled to the third power supply.

10. The circuit of claim 8, the fourth transistor further comprising an electrode coupled to the second power supply.

11. The circuit of claim 8 further comprising a different node disposed between the third and fourth transistors, wherein a voltage level at the different node is pulled to the second voltage level in response to the first state of the input signal, and pulled to the third voltage level in response to the second state of the input signal.

12. A circuit for converting voltage levels comprising:

an input signal having a first voltage level and a second voltage level;

a first transistor including a gate electrode for receiving the input signal;

a second transistor including a gate electrode for receiving a bias voltage;

a current source providing a current in response to the first voltage level of the input signal; and

a node disposed between the second transistor and the current source;

wherein the second transistor clamps a voltage level at the node between a third voltage level and a fourth voltage level; and

wherein the voltage level at the node is approximately the third voltage level in response to the first voltage level of the input signal, and approximately the fourth voltage level in response to the second voltage level.

13. The circuit of claim 12, the first transistor, second transistor and current source being formed between a first power supply providing the second voltage level and a second power supply providing the third voltage level.

14. The circuit of claim 12, the bias voltage being approximately the fourth voltage level plus a gate-to-source voltage of the second transistor.

15. The circuit of claim 12, the current source further comprising a current mirror generating the current.

16. The circuit of claim 12 further comprising a complementary inverter formed between a third power supply providing the fourth voltage level and the second power supply providing the third voltage level.

17. The circuit of claim 16, the complementary inverter further comprising a third transistor including a gate electrode coupled to the node, and a fourth transistor including a gate electrode coupled to the node.

18. The circuit of claim 17 further comprising a different node disposed between the third and fourth transistors, wherein a voltage level at the different node is approximately the third voltage level in response to the first voltage level of the input signal, and approximately the fourth voltage level in response to the second voltage level of the input signal.

19. The circuit of claim 12, the first and second transistors including high-voltage transistors.

20. A method for converting voltage levels comprising:

providing a first power supply of a first voltage level;

providing a second power supply of a second voltage level;

forming a first transistor between the first and second power supplies including a gate electrode;

providing to the gate electrode of the first transistor an input signal including a first state and a second state;

forming a second transistor between the first transistor and the second power supply including a gate electrode;

providing to the gate electrode of the second transistor a bias voltage;

forming a current source between the second transistor and the second power supply providing a current in response to the first state of the input signal;

pulling a voltage level at a node disposed between the second transistor and the current source to a third voltage level in response to the first state of the input signal; and

pulling the voltage level at the node to the second voltage level in response to the second state of the input signal.

21. The method of claim 20 further comprising pulling a different voltage level at a different node disposed between the first transistor and the second transistor in response to the first state and the second state of the input signal.

22. The method of claim 20 further comprising:

providing a third transistor including a gate electrode coupled to the node; and

providing a fourth transistor including a gate electrode coupled to the node.

23. The method of claim 20 wherein the bias voltage clamps the voltage level at the node.

24. The method of claim 20, the bias voltage being approximately the third voltage level plus a gate-to-source voltage of the second transistor.

25. The method of claim 20 further comprising providing a complementary inverter.